CpE 6220

Design Automation of VLSI Systems

Final Project Report

Implementation of Placer

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**1. Objective:**

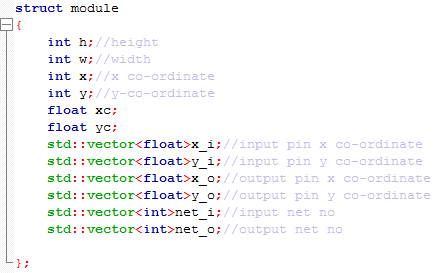
To design a placer to minimize the Half Perimeter Wire Length(HPWL) given number of modules and netlist as input.

**2. Methodology:**

**a. Parsing:**

The first step done is clustering. The data from the benchmark files is parsed and is organized into two structures.

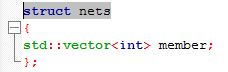
**i. struct module:**



Each module height, width, x and y position , all x and y coordinates of the input and output pins, the number of input output nets is organized in this structure.

Then based on the module position and the width and height of each module the centre coordinates of each module were calculated .

**ii. struct nets:**

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The data regarding the modules present in each net is organized in this structure.

**b. Clustering:**

The second step done is clustering. Groups of three fixed modules were considered and then all the modules connected with these fixed modules were grouped as one cluster. The same process was repeated for all the fixed modules.

**c. Quadratic Placement**

The third step done is quadratic placement. Once clustering is done then Quadratic Placement algorithm is applied for each of the cluster.

First connectivity Matrix C is prepared based on the weights connected between the movable modules in the cluster. Then Matrix A is prepared by taking the negative of matrix C and then diagonal elements are the sum of weights of all the modules(including fixed module) connected to a particular fixed module.

Matrix Bx is prepared based on the product of x coordinate of fixed module and the corresponding weight connected to the movable module. If a movable module is connected to multiple fixed module then the sum of them is taken.

Similarly Matrix By is prepared based on the product of y coordinate of fixed module and the corresponding weight to the movable module.

All the weights between the modules are considered as 1.( as it is given that all the weights are equal)

Then the equations A.X=Bx and A.Y=By are solved using Intel Math Kernel Library (MKL).

We used the below functions:

dgetrf( ): Used to generate LU decomposition of a general matrix.

dgetri( ) : Used to generate inverse of a matrix for a LU decomposition matrix

dgemm( ): Used to Mulitply two matrices.

By solving these equations we got the placement positions of the movable modules.

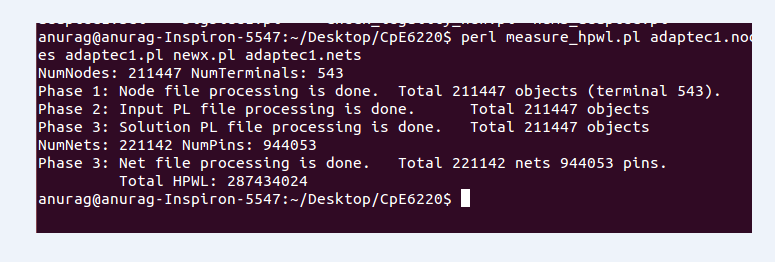
**d. Row positioning:**

Once we got the x,y positions of the movable modules then the modules off the row were placed into the row each of height 12 according to the .scl file.

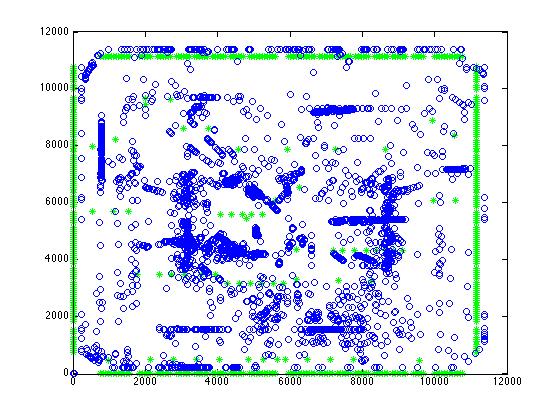
**3. Results:**

Adaptec 1 file :-

HPWL :- 287184662



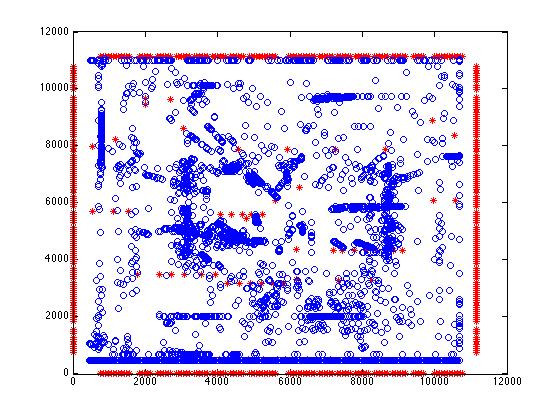
Before Row Positioning :-



Green points :- fixed modules, which are represented in a point

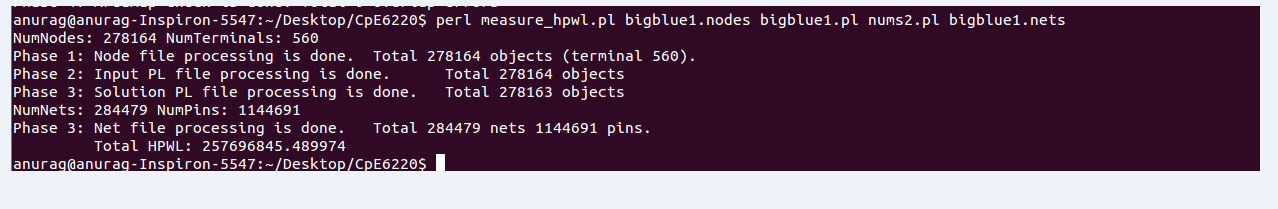
Blue points :- Movable modules, which are represented in a point

After Row Positioning :-

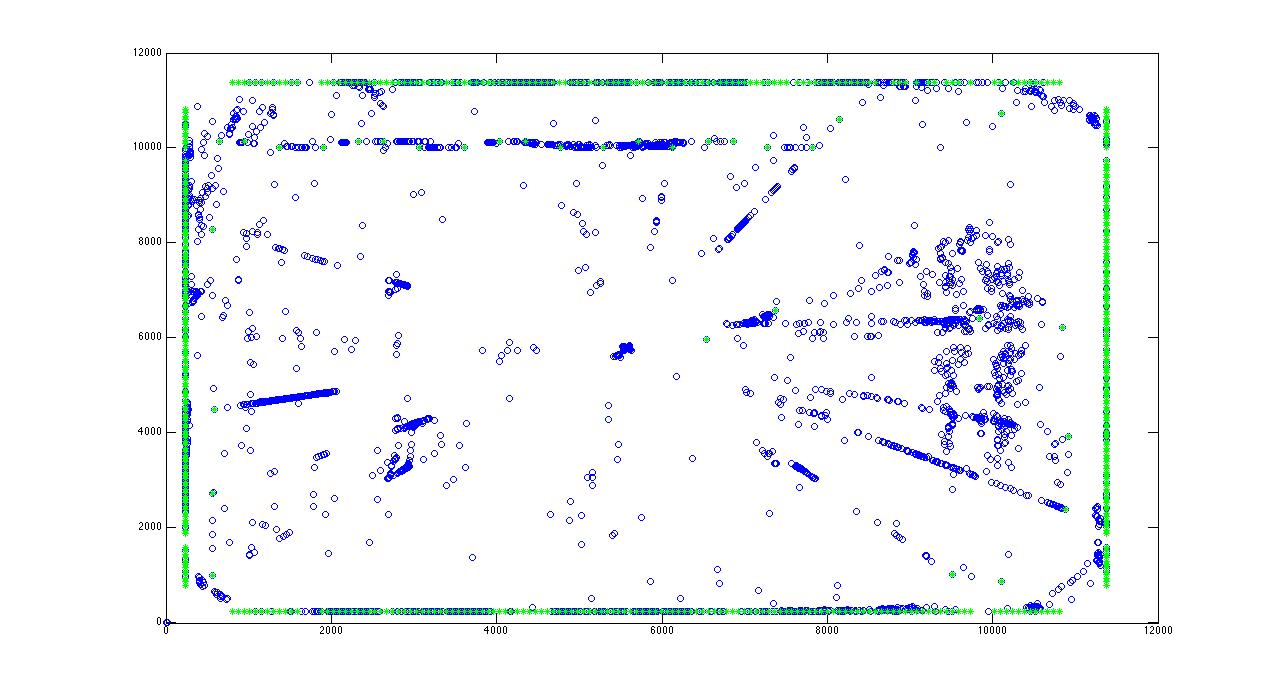


Big Blue 1 file :-

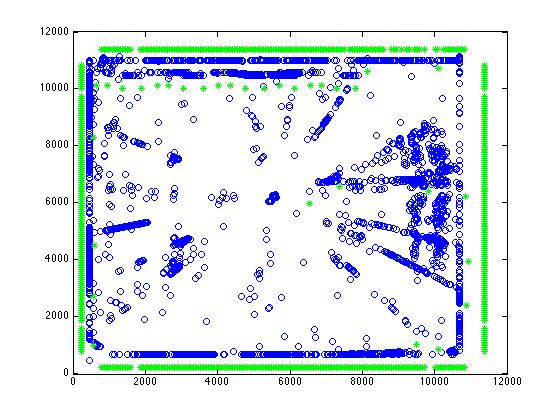
HPWL :- 257696845



Before Row Positioning :



After Row Positioning :



Conclusion

We could completely do parsing, clustering, quadratic placement, and row positioning for the above modules and could achieve reasonable HPWL, but regarding legalization we could achieve this completely.